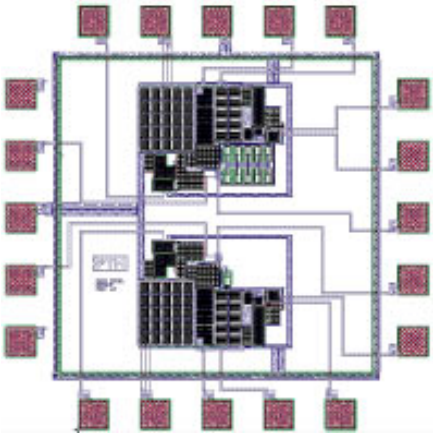

Fig. 5.16: 1996 0.8 μ BiCMOS preamplifier.

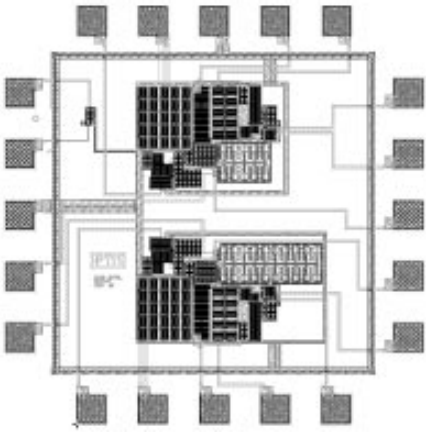

Fig. 5.17: 1997 0.8 μ BiCMOS preamplifier.

5.7 Floating-Point ADC

The floating-point readout scheme, described in Section 5.3, makes use of a commercial analog-to-digital converter (ADC), along with a custom chip that performs the gain selection before the ADC. This custom circuit (called the 'Floating-Point Unit' or FPU) is described in Subsection 5.7.1, and the ADC in Subsection 5.7.2.

5.7.1 Floating-point signal acquisition circuit

The FPU [5.7] is shown schematically in Fig. 5.18. The two preamplifier outputs ($\times 1$ and $\times 8$, with clamp) are each followed by two amplifiers of gain 1 and 4 (also with clamps). These amplifiers (which were external, commercial op-amps for the 96/X3 and *Proto97* tests) create four outputs ($\times 1$, $\times 4$, $\times 8$ and $\times 32$), each with a programmable pedestal offset. (The unity gain amplifiers are present to perform the offset function and minimize phase delay between the outputs.) The four outputs serve as the analog inputs to the FPU. The (at present) external gain stages are being integrated into the preamplifier in order to minimize noise and power consumption.

The FPU chip consists of four sample/holds, comparators, digital logic, multiplexers and a final buffer to drive the signal off chip to the ADC. Two clocks, each at 40 MHz are employed. The first clock (SCLK) controls the sample/hold transitions, and a second clock (MCLK) controls the internal logic which determines the multiplexer output.

The FPU operates in the following way. Every 25 ns, the four amplified inputs are stored by the sample/holds. After the propagation delay of the comparators (which compares the signal level to a common externally provided threshold), the comparator outputs become valid. Digital logic is then employed to select the highest gain signal which is below the threshold. When MCLK is applied, the selected channel is multiplexed out. After the ADC conversion begins, the sample/holds return to sample mode. Additional digital logic is provided to be able to 'force' a particular output for test or calibration. For the '97 FPU, an internal self-calibration feature has been added. This feature would be used in special calibration runs in order to verify the inter-stage gains as described below.

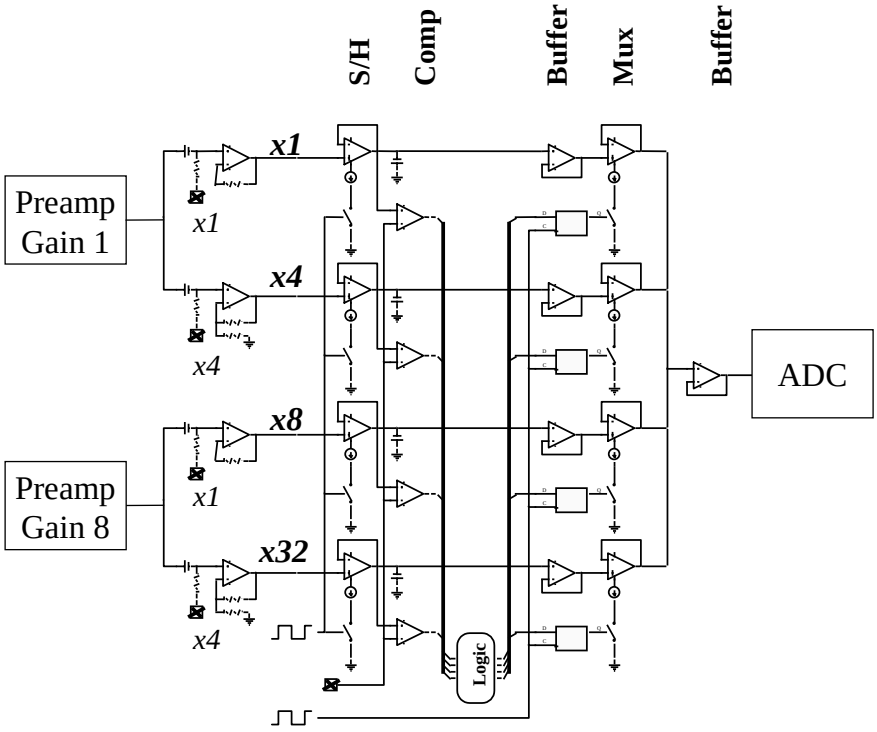

Fig. 5.18: Floating-point unit schematic.

Two different FPUs were produced and tested for the 96/X3 tests: one version in 0.8 μ BiCMOS (shown in Fig. 5.19 and Fig. 5.20), and the other in 0.7 μ *CHFET* (shown in Fig. 5.21), which is a *complementary* GaAs process. Although the two devices were functionally the same, the internal design was quite different, owing to the differing possibilities and restrictions of the technologies. The BiCMOS performance was superior to that of the *CHFET* circuit (at the expense of significantly higher power consumption). BiCMOS is thus a natural candidate for the final implementation. The experience with *CHFET*, however, will prove valuable in the fibre-optic readout development, described in Section 5.8.

The self-calibration feature of the *Proto97* 0.8 μ BiCMOS FPU is depicted in Fig. 5.22. In this mode, the two clocks (the sample/hold and the multiplexer decision clock) operate at different frequencies. The sample/hold operates once out of every two clock cycles (i.e. a signal is acquired every 50 ns). On the acquisition cycle, the FPU operates normally. On the subsequent cycle, however, the sample/hold remains in hold so that the same analog signal level as before is used. Depending on a downloaded code, the same gain range (n_1), the next lowest gain range ($n_1 + 1$), etc., is multiplexed to the ADC. The *Proto97* FPU is ~ 6 mm^2.