A Large Ion Collider Experiment







## Upgrade of the ALICE Inner Tracking System



ALICE | Rencontres QGP-France 2014 | 15-18/9/2014 | Levente Molnar (CNRS IPHC) for the ALICE Collaboration

## OUTLINE



- ALICE Upgrade strategy and the ITS project
- Detector and physics performance à la TDR
- Pixel chip technology
- ITS Upgrade activities at Strasbourg



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# ALICE

## ALICE UPGRADE STRATEGY

Physics program requires 10 nb<sup>-1</sup> of integrated luminosity of Pb-Pb collisions wrt. the approved program of 1 nb<sup>-1</sup>

## Physics signals of interest are rare, mostly not triggerable

- Low  $p_T$  (below 1 GeV/c), high combinatorial background
- Increase rate capabilities for minimum bias heavy-ion collisions to 50 kHz – 100 kHz

#### ALICE runs at high luminosity

- Factor 100 increase in statistics (for untriggered probes)
- Requires smaller beam pipe, <u>new detectors</u>: <u>ITS</u>, <u>MFT</u>, upgraded TPC read-out chambers and readout electronics upgrade for other detectors
- New combined online-offline framework: O<sup>2</sup>

#### Preserve ALICE uniqueness

– Low  $p_T$  measurements and particle identification

## Upgrade in the 2nd LHC Long Shutdown (LS2) 2018/19





## Full list and details of upgrade strategy: ALICE LoI, CERN-LHCC-2012-012

### **MOTIVATION FOR A NEW INNER TRACKING SYSTEM**



- move closer to IP (position of first layer): 39 mm  $\rightarrow$  22 mm
- reduce material budget  $X/X_0$  / layer: from ~1.14% ...
  - ... to 0.3% (inner layers) and to 0.8% (outer layers)
- reduce pixel size: 50  $\mu$ m × 425  $\mu$ m $\rightarrow$ O(30  $\mu$ m × 30  $\mu$ m)
- Improve tracking efficiency and  $p_{T}$  resolution at low  $p_{T}$ 
  - increase granularity: 6 layers  $\rightarrow$  7 layers
- Fast readout (now limited at 1 kHz with full ITS):
  - Pb-Pb: up to 100 kHz
  - pp: several 100 kHz
- Fast insertion/removal
  - possibility to access for yearly maintenance

The new ALICE ITS will fully replace the present ITS !



- Project approved by LHCC in Sept. 2012
- Technical Design Report approved by LHCC in Dec 2013
- Budget approved by CERN Upgrade Cost Group / Research Board in March 2014
- Decision on pixel chip architecture: Q2 / 2015 (tbc)
- Enter production phase in 2016 ٠
- Installation commissioning 2018/2019 ٠

French Institutes (CNRS-IN2P3) in the project: IPHC+Univ. (Strasbourg), LPSC+Univ. (Grenoble) Upgrade of the

Inner Tracking System

CERN-LHCC-2013-024; ALICE-TDR-017





TDR

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## Present and upgraded ITS performance





- Standalone tracking efficiency ~ 70 % at p = 100 MeV/c
- Improvement in momentum resolution for standalone tracking





### SUMMARY OF ITS UPGRADE PHYSICS REACH (TDR)

	Current, $0.1 \mathrm{nb}^{-1}$		Upgrade, $10 \mathrm{nb}^{-1}$	
Observable	$p_{\mathrm{T}}^{\mathrm{min}}$	statistical	$p_{\mathrm{T}}^{\mathrm{min}}$	statistical
	(GeV/c)	uncertainty	(GeV/c)	uncertainty
Heavy Flavour				
D meson $R_{AA}$	1	10%	0	0.3%
$D_s meson R_{AA}$	4	15%	< 2	3%
D meson from B $R_{AA}$	3	30%	2	1%
${ m J}/\psi$ from B $R_{ m AA}$	1.5	$15\%$ (p_T-int.)	1	5%
$B^+$ yield	not accessible		3	10%
$\Lambda_{ m c}  R_{ m AA}$	not accessible		2	15%
$\Lambda_{\rm c}/{\rm D}^0$ ratio	not accessible		2	15%
$\Lambda_{\rm b}$ yield	not accessible		7	20%
D meson $v_2 (v_2 = 0.2)$	1	10%	0	0.2%
$D_{\rm s} {\rm meson} v_2 (v_2 = 0.2)$	not accessible		< 2	8 %
D from B $v_2 (v_2 = 0.05)$	not accessible		2	8 %
$J/\psi$ from B $v_2 \ (v_2 = 0.05)$	not accessible		1	60%
$\Lambda_{\rm c} v_2 \ (v_2 = 0.15)$	not a	accessible	3	20%
	Dielectro	ns		
Temperature (intermediate mass)	not accessible			10%
Elliptic flow $(v_2 = 0.1)$ [4]	not accessible			10%
Low-mass spectral function [4]	not a	accessible	0.3	20%
	Hypernuc	elei		
$^{3}_{\Lambda}$ H yield	2	18%	2	1.7%

Pb–Pb collisions for an integrated luminosity of 10 nb<sup>-1</sup>

#### Improving precision

## Access to new observables

ALICE, CERN-LHCC-2013-024



#### PHYSICS PERFORMANCE, PARTICLE PRODUCTION



Newly accessible heavy baryons/mesons in Pb-Pb

Pb-Pb, 5.5 TeV, Minimum-bias and 0–10 % central collisions, 10 nb<sup>-1</sup>



12

14

p<sub>\_</sub> (GeV/c)

10

16

## PHYSICS PERFORMANCE, ENERGY LOSS



Significant reduction of uncertainties, new heavy baryons/mesons in Pb-Pb collisions

Pb-Pb, 5.5 TeV, 0–10 % central collisions, 10 nb<sup>-1</sup>







## PHYSICS PERFORMANCE, HADRONIZATION, FLOW



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#### PHYSICS PERFORMANCE, DI-LEPTONS Excess after background subtraction



Estimation of the temperature at various phases of system expansion with 10-20% precision (stat.+syst.)



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## LAYOUT OF THE UPGRADED ITS

- 7 layers layout:
  - 3 layers of Inner Barrel
  - 4 layers of Outer Barrel
- Radial coverage: 22 mm to 400 mm
- η coverage: |η| ≤ 1.22, for tracks from 90 % most luminous region



- ~ 12.5 Gigapixels, binary readout
- ~ 10 m<sup>2</sup> of silicon



 Expected radiation level (innermost layer, including a safety factor 10): 700 krad (TID) and 1 × 10<sup>13</sup> 1 MeV n<sub>eq</sub> (NIEL)

## PIXEL TECHNOLOGY

- Requirements:
  - very thin sensors
  - very high granularity
  - cover large area
  - withstand modest radiation level
- Choice:
  - monolithic silicon pixel sensors using TowerJazz 0.18 µm CMOS Imaging Process
    - high-resistivity (1-6 kΩcm) epitaxial layer on p-type substrate
    - deep p-well to shield PMOS: true CMOS circuitry in the pixel





ALICE, CERN-LHCC-2013-024

Nwell diode output signal: V ~ Q/C

- minimize charge spread over different pixels
- minimize capacitance
- small diode surface (~ 100x smaller than pixel area) and large depletion volume
- Moderate bias voltage on the substrate can increase depletion zone around the Nwell charge collection diode



## PIXEL CHIP VERSION UNDER DEVELOPEMENT

#### ALICE, CERN-LHCC-2013-024



- Three pixel chip architectures under development: MISTRAL / ASTRAL and ALPIDE
- Decision on the ALICE Pixel Chip architecture for the ITS Upgrade: Q2 / 2015 (tbc)

#### Specifications:

- Chip size: 15 mm x 30 mm
- Pixel pitch: ~ 30 µm
- Si thickness: 50 µm
- Spatial resolution: ~ 5 µm
- Power density: < 100 mW/cm<sup>2</sup>
- Integration time: < 30 µs



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## **ITS UPGRADE ACTIVITIES IN STRASBOURG**

- Pixel chip R&D (PICSEL group)
  - Pixel chip development and test: MISTRAL/ASTRAL
- Outer Barrel module production (ALICE + Micro-techniques groups)
  - Preparation for assembly
- **ITS Upgrade software** (ALICE group)
  - Framework coordination
  - Standalone reconstruction framework
  - Pixel chip response simulation
- Physics performance analysis (ALICE group)
- Editorial work: ITS Upgrade TDR (ALICE + PICSEL groups)

MIMOSA34

## **IPHC: MISTRAL / ASTRAL DEVELOPMENT**

Several small scale prototypes have been realized and characterized ...

MIMOSA-34 MIMOSA-32FEE MIMOSA-22THRA MIMOSA-22THRB \* sensing node & pixel dimensions \* in-pixel circuitry & end-of-col. discri. \* double-row read-out

... fulfilling the ALICE ITS specifications (SNR, radiation hardness, ...)

.. and leading to the FSSBs (Full Scale Building Block = 1/3 of a full chip)



- FSBBs received in late Q2/2014
  - Currently characterized in lab:
    - Fabrication yield
    - Uniformity of chips
- Test beam at CERN SPS: Oct 2014









CDS: correlated

### PIXEL CHIP R&D ASTRAL / MISTRAL – MIMOSA-34



- Analogue, no in-pixel pre-amplification and CDS circuitry
  - double sampling sensing node optimisation: pixel size, epitaxial layer characteristics
- Pixel size varies from 22 × 27  $\mu m^2$  to 22 × 66  $\mu m^2$
- High detection efficiency even for large 22 × 66  $\mu$ m<sup>2</sup> pixels
  - $\rightarrow$  Favourable pixel option for Outer Barrel

## **IPHC: OUTER BARREL MODULE ASSEMBLY**



The ITS project identified the following module assembly sites: CERN, LBNL, STFC, CCNU, INFN, IPHC, Korea, Netherlands, Thailand

IPHC is committed to assemble 200-250 out of 1250 modules of the OB

Start of module assembly: 2016, 1 module built and tested / day



**Outer Barrel Stave** 

## **IPHC: MODULE ASSEMBLY PREPARATION**

#### 2014/06

- Adapt the ALICE module assembly procedure to the local infrastructure
- Improvements: automatic placement and alignment of chips, (interfaced) automatic vacuum control

Planned activities for 2014/Q4 - 2015/Q2

- Tools manufacturing at IPHC
- Preparation of positioning and vacuum control protocols
- Dummy module assembly: placement, gluing, soldering / laser soldering training

#### Planned activities for 2015/Q3 - 2016

- Training on common automatic assembly machine and its procurement
- Start of production in 2016 ...





#### ZEVAC IP500 (precision ~ 5 μm)

### SUMMARY



- The new ALICE ITS with 7 layers of monolithic silicon pixel detectors will be installed during LS2 of the LHC in 2018/19 completely replacing the present ITS
- Full-scale chip prototypes are currently being characterized leading to a decision on the ALICE Pixel Chip architecture for the ITS Upgrade around 2015 / Q2
- ITS Upgrade activities at IPHC: chip R&D, simulation + reconstruction software, physics performance analysis are extended with the preparation for module assembly