Multi gigabit transceiver (Virtex2Pro), with reduced latency.
Measurements of Bit Error Rate versus clock jitter.

T. ROMANTEAU – LLR / IN2P3

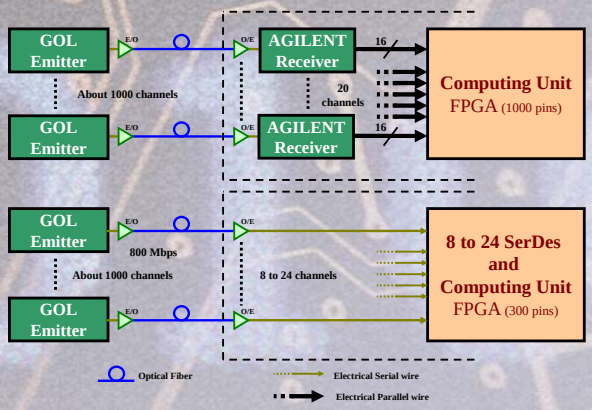
Laboratoire Leprince Ringuet
Ecole polytechnique – IN2P3/CNRS

Embedded Serial Link

Multi Giga-Bit Transceivers (MGT) embedded in the Virtex2Pro FPGA from XILINX is a key technology to reduce the overall cost of ECAL/CMS electronics:

- **Less components** ➔ *smaller PCB, less power consumption, better reliability.*
- **Less wires** ➔ *simpler PCB design, less pins on package, lower cost FPGA.*
- **SerDes and computing unit embedded in the same package** ➔ *faster speed, better signal integrity.*

Compared Solutions

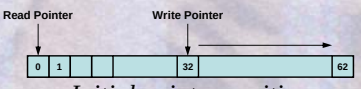


Reducing the Latency of MGT, a solution for ECAL?

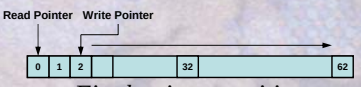
In the MGT standard primitive the latency is about 25 clock cycles and does not satisfy the CMS experiment ECAL/Trigger requirements.

The MGT custom primitive can be used to reduce the latency to 8 clock cycles. This solution consists of shifting the writing pointer of the internal elastic FIFO buffer during the reset initialization phase.

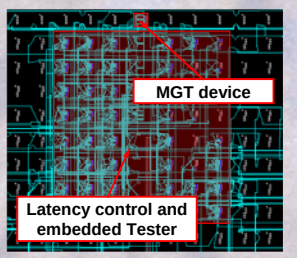
- This solution is directly applicable for the LHC experiments thanks to their clock specific synchronous distribution scheme (see below the clock jitter margin as measured in this condition).
- ***Consequently, this more integrated solution could provide an economic alternative to the current approach based on discrete transceivers,*** but needs a review of the latency budget for the trigger data path.
- This latency reduction has been checked by XILINX on a single channel and is under development at LLR on a multi channel setup.



Initial pointer position

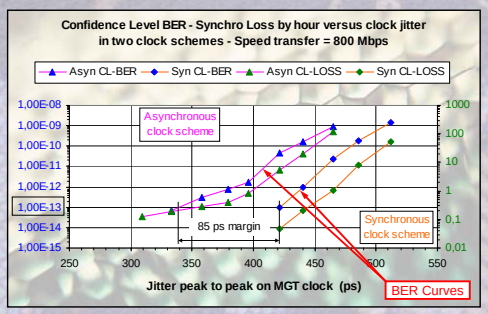


Final pointer position



Physical implantation

Jitter margin effect of the distribution clock scheme



Measurement of Bit Error Rate versus clock jitter with two clock distribution scheme

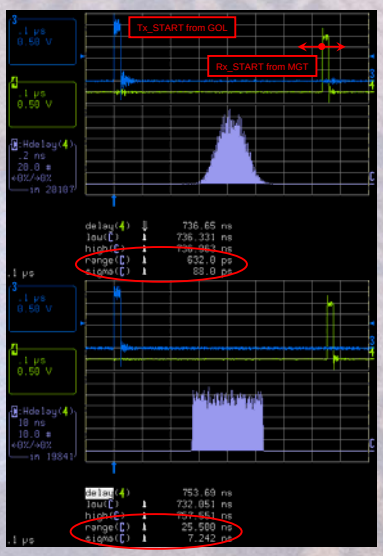
In a previous project phase, a BER test platform developed by Xilinx Design Services (see LHCC-G-014) was used to study the GOL- MGT connection. This platform has been reused to study the effects on the BER of the LHC clock jitter. The tests were performed with a 800 Mbit/s link speed.

Using a programmable calibrated jitter (below), the testing platform provides a direct measurement of the BER and the synchronization loss. The results (left) exhibit for the LHC clock scheme :

- ***A clock jitter margin of 85 ps***
- ***Latency relatively insensitive to the jitter***

Latency jitter effect of the distribution clock scheme

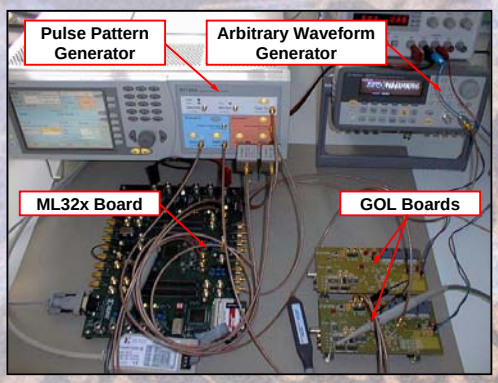
Synchronous system clock



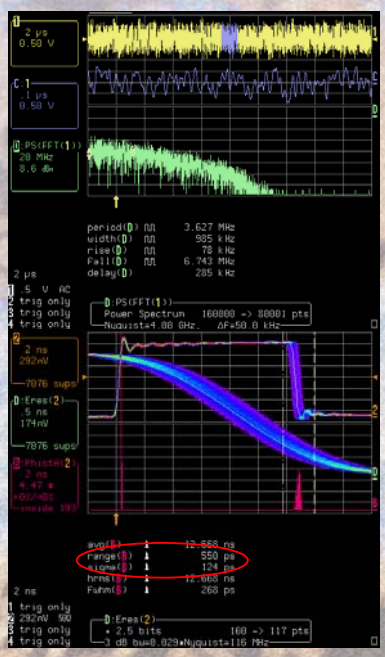
Asynchronous system clock

BER testing platform

- MGT testing board (ML320 from XILINX)
- Pulse Pattern generator (AGILENT 81134A)
- Arbitrary Waveform generator (AGILENT 33250A)
- GOL test board from CERN
- LECROY scope (SDA6000 or LC584M)



Noise Source Characterization



40 Mhz clock with injected jitter